IN THE SPECIFICATION:

Page 3, line 13, please amend as follows:

In inverter circuits IV0 - IV4, MIS transistors P0, P2 and P4 are ~~off~~ on, and therefore do not cause a sub-threshold leak (off-leak) current. Meanwhile, MIS transistors P1 and P3 are off, and cause an off-leak current from sub-power supply line SVL. The off-leak currents flowing through MIS transistors P1 and P3 flow to main ground line MGL through MIS transistors N1 and N3 in the on state, respectively. However, the off-leak current flowing through MIS transistors P1 and P3 depends in magnitude on the off-leak current flowing through switching transistor SWP. Therefore, the voltage level of sub-power supply line SVL reaches an equilibrium state where the off-leak current flowing through switching transistor SWP is balanced with the sum of off-leak currents flowing through MIS transistors P1 and P3. Due to the current flow, the voltage level of sub-power supply line SVL is lower than power supply voltage VCC, and MIS transistors P1 and P3 enters such a state that the gate to source thereof is reverse-biased, and therefore enters a deeper off state. Accordingly, MIS transistors P1 and P3 can have the off-leak currents sufficiently reduced.